REMARKS

Objections to the drawings:

The Examiner objected to the drawings for not including particular reference signs mentioned in the description. However, these reference signs are included in the drawings including in at least the following places:

"Applications software 1 through N" are illustrated in FIG. 1 including applications software 1 identified by reference number 20 and applications software 2 through N identified by reference number 24.

"Processors 1 through N" are illustrated in FIG. 1 including processor 1 identified by reference number 12 and processors 2 through N identified by reference number 14.

Reference number 30 is included in FIG. 2.

The specification is being amended to clarify the correspondence between the reference numbers used in the specification and the reference numbers used in the drawings.

Objections to the specification:

The Examiner stated that the abstract is more than 150 words and that appropriate action is required. Applicant has deleted the text appearing after the abstract, thus the abstract is now less than 150 words.

§102 Rejections:

The Examiner rejected claims 1-18 under 35 U.S.C. §102(b) as being anticipated by Geoffrey J. Bunza (U.S. 5,838,948).

Claims 1-18 are patentable over Bunza, since Bunza neither describes nor suggests at least "providing a first processor on a single silicon chip; loading, on the first processor, a software simulation of a second processor that is to be provided in hardware on the single silicon chip," as recited in claim 1. Bunza also neither describes nor suggests to, "configure a software simulation of a first processor, which is to be provided in hardware on a single silicon chip, to execute on a second processor on the single silicon chip," as recited in claim 10, or "a first

processor on a single silicon chip having loaded thereon, a software simulation of a second processor that is to be provided in hardware on the single silicon chip," as recited in claim 17.

The Examiner states that Bunza teaches "providing a first processor on a single chip; loading, on the first processor, a software simulation of a second processor that is to be provided in hardware on the single silicon chip" and appears to identify "first and second target microprocessors" described by Bunza at col. 2, lines 52-55 as the first and second processors. The Examiner further identifies block 100 in Bunza's FIG. 5 as "hardware of the microprocessors." However, processor chip 100 in FIG. 5 is not described as hardware for Bunza's "first and second target microprocessors" since FIG. 5 is part of a section that is "a brief discussion of conventional simulation systems [that] serve to distinguish the present invention," (col. 5, lines 41-42) and Bunza's "first and second target microprocessors" are described as being included in an "embodiment" of the invention. Nowhere does Bunza teach or suggest that the first and second target microprocessors are on a single silicon chip.

Furthermore, neither does Bunza teach "loading, on the first processor, a software simulation of a second processor," or "executing the software simulation of the second processor and the applications software on the first processor," as recited in claim 1. Instead, Bunza describes:

> ...the system includes first and second target microprocessors each having a memory storing a set of computer instructions to be executed on the respective target microprocessors. In this embodiment, the communications interface controls communication from the first and second processor emulators to the hardware simulator. The first and second processor emulators communicate with the first and second memories, respectively, to receive the first and second sets of computer instructions therefrom. (col. 2, lines 52 –61)
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> *** In another embodiment of the system 200, multiple processor emulators 202 can support simultaneous target programs executing concurrently, as illustrated in FIG. 9. Each processor emulator 202 maintains synchronization locally and executes its own target program 22 (see FIG. 6). If one processor emulator 202 is waiting

for something to happen, this does not prevent another processor emulator from executing independently. (col. 16, lines 23-30)

Bunza's description of "computer instructions" does not suggest instructions to execute a software simulation of the one processor on another processor. To the contrary, Bunza describes each processor emulator executing its own target program independently. Therefore, claims 1, 10 and 17 are patentable.

Other claims further distinguish over Bunza. For example, dependent claim 2 further distinguishes over Bunza by requiring that "the software simulation of the second processor includes a slow, highly detailed simulation of the second processor and a fast, high-level simulation of the second processor." The Examiner states that Bunza teaches this at col. 11, lines 47-67 and particularly identifies the high speed "processor emulator" as the fast, high-level simulation included in the software simulation of the second processor. However, at col. 11, line 49 Bunza describes "processor emulator 202" as "a high speed hardware device." Therefore, Bunza does not disclose these features of claim 2.

Dependent claims 2-9 depend on claim 1, dependent claim 11 depends on claim 10, and dependent claim 18 depends on claim 17, and are therefore patentable for at least the same reasons as for claims 1, 10 and 17.

Similarly, Bunza does not disclose or suggest "loading, on a first processor, a plurality of software simulations of a plurality of second processors that are to be provided in hardware on a single silicon chip," as recited in claim 12. As argued above, Bunza does not teach that any of a plurality of processors are provided in hardware on a single silicon chip. Neither does Bunza teach "loading, on a first processor, a plurality of software simulations of a plurality of second processors." Therefore, claim 12 is patentable.

Dependent claims 13-16 depend on claim 12, and are therefore patentable for at least the same reasons as for claim 12.

Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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